ABSTRACT

DIGITAL PULSE-WIDTH-MODULATION GENERATOR

A digital pulse-width-modulation (PWM) generator comprising:

an n bit digital magnitude comparator having first and second n bit inputs and an output indicative of the relative values of the signals applied at the first and second inputs;

a first n bit digital up/down counter having a count direction input coupled to receive a sign bit of a digital unary input signal, an n bit parallel binary count output connected to the first n bit input of the magnitude comparator, and a clock input;

a second n bit counter having a clock input coupled to receive a constant rate clock signal and an n bit parallel binary count output connected to the second n bit input of the magnitude comparator;

an AND gate having a first input coupled to receive the constant rate clock signal in frequency divided form and a second input coupled to receive a magnitude portion of the digital unary input signal, and further having an output connected to the clock input of the first counter; and

wherein the comparator continually generates an output signal indicative of the relative magnitudes of the counts of the first and second counters, whereby said output signal is a PWM output signal with an average value representing a ramp voltage having a slope determined by magnitude portion of the digital unary input signal with a direction of a slope of the output signal being determined by the polarity of the sign bit.